NON-VOLATILE AND-TYPE CONTENT ADDRESSABLE MEMORY

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to semiconductor memories and, more

5   particularly, a non-volatile content addressable memory (CAM).

Description of the Related Art

As is known, semiconductor memories, such as used in microprocessors, personal computers, ASIC's, and the like, consist of a large number of cells arranged in rows and columns to form a cell matrix. Each cell

10   contains a binary information element (bit) and to each row of the matrix there corresponds a binary word whose length depends on the number of columns.

At present the most widely used memories are the static or dynamic RAMs (Random Access Memories) in which the word memorized in a row of the matrix can be accessed by simply furnishing its address. In the case of a CAM cell

15   matrix, on the other hand, a binary word stored in a row can be searched by inserting the word to be found in a comparison register associated with the matrix and comparing the content of the comparison register with the content of each row. The result of the search is made available by means of the observation of the voltage of a match line common to all the cells of a row. In a cell matrix, obviously,

20   this operation is carried out simultaneously for all the binary words of each row. In other words, a content addressable memory is accessed by means of a comparison with its specific content rather than by means of a specific address.

There exist both volatile CAM cells and non-volatile CAM cells. The volatile CAM cells were initially developed from static RAM cells (SRAM) by simply

25   adding transistors in such a manner as to provide an output connected to a match

line. More recently, dynamic RAM cells (DRAM) have also been used as basic cells to obtain advantages in terms of area and cost.

CAM cells, irrespective of whether they are made with SRAMs or DRAMs, are relatively fast, but their binary content is lost as soon as the supply

5　voltage is switched off. They therefore have to be rewritten at every new start-up by using a separate non-volatile memory unit, a hard disk for example. In CAMs of a non-volatile type, on the other hand, the data remain stored even when the voltage is cut off and, what is more, each cell calls for a smaller number of transistors and therefore a smaller silicon area than cells realized with SRAMs and

10　DRAMs.

A known non-volatile content addressable memory cell 210, as described - for example - in U.S. Patent No. 6,317,349 B1 and shown in Figure 1 of the drawings attached hereto, comprises two transistors 211,212 of the floating-gate type that have their gate terminals connected to the same word line (WL) 220,

15　their source terminals both connected to a match line (ML) 230 and their drain terminals each connected to one of the bit lines (BL, BL) 241,242. In general, any non-volatile memory element could take the place of the two transistors. A multiplicity of cells equal to the cell 210 of Figure 1, ordered in rows and columns, forms a content addressable memory matrix, schematically represented in Figure

20　2, where each row of cells comprises a pair of electric lines, respectively a word line 220 and a match line 230, and each column comprises two bit lines indicated by 241,242.

All the word lines 220 are connected to an external row control block 360, the match lines 230 have one of their ends connected to this same block 360,

25　while at the other end they terminate in sense amplifiers 380. Pilot circuits 371 and 372 are coupled, respectively, with the bit lines 241 and 242 to bias them during the search, writing, and cancelling operations. All the bit lines of the matrix lead to a block 370 that performs the function of register and control circuit for the search. The block 370 may contain a word for comparison purposes that is

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applied to its terminal indicated by DATA IN. The line control block 360 applies adequate voltages to the word lines and the match lines during the search, writing, and cancelling operations by selecting one row of the cell matrix on the basis of an input signal ADRIN. The sense amplifiers 380 detect a voltage variation on the

5   respective match lines 230 when the input word, contained in block 370, does not coincide with the word memorized in the corresponding row of the matrix.

The threshold voltage of the transistors 211,212 can be modified by acting on the terminals thereof to vary the electric charge of the respective floating-gates. The threshold voltage is "low" and determined by technological and design

10   parameters when electrons are not accumulated in the floating-gate transistors and "high" when they are being accumulated. The high threshold voltage is fixed at a value greater than the supply voltage Vcc of the memory circuits (for example Vcc=5V), while the low voltage, as a general rule, is not greater than 1 V. Conventionally, when the threshold voltage of the transistor 211 is set high, while

15   that of transistor 212 is set low, the elementary information stored in the cell 210 is a logic 1. When the thresholds are set in the opposite manner, a logic 0 is memorized. It is also possible to memorize a third state X, known as the don't care state, by programming the thresholds of both non-volatile elements to be high (>Vcc). The associative memories capable of memorizing these three states,

20   rather than just the two basic logic states, are known as ternary memories. They are particularly advantageous in some applications.

Before undertaking the programming, the information content of the cell is cancelled by applying a sufficiently negative voltage to the word line 220 (for example, from −8V to −10V) and a positive voltage to the match line 230 (for

25   example from 5V to 7V). The combination of these voltages on the gate and source terminals of the transistors 211,212 causes a tunnel effect capable of removing electrons from the floating gate of the transistor that has the high threshold voltage and thus reducing it to the low threshold voltage. This operation exerts an effect (of lesser entity) also on a transistor already set to a low threshold

voltage. One therefore needs appropriate algorithms to re-program the cells that have had their thresholds excessively lowered and thus obtain a well controlled final value. The value of the voltage on the bit lines 241,242 does not exert any effect on the cancellation.

5   The operation of writing a CAM cell 210 is carried out by applying a high voltage to the word line 220 (for example, 8V) and setting the match line at ground voltage. When a logic 1 is to be memorized, the threshold of transistor 211 has to be stepped up, leaving the threshold of transistor 212 low, and an intermediate voltage (5V, for example) is applied to the bit line 241, leaving the

10   other bit line 242 unconnected. To memorize a logic 0, on the other hand, one operates on the bit lines in the opposite manner to raise the threshold of transistor 212. When the don't care state X has to be memorized, the intermediate voltage is applied to both the bit lines 241 and 242.

The search operation in the cell 210 is performed by applying a

15   supply voltage V_{CC} to the word line 220, pre-charging the match line 230 with the voltage V_{CC} and applying appropriate voltages to the bit lines 241,242. In particular, when the memorized data is a logic 1 (threshold of 211 high, threshold of 212 low) and the same bit is looked for in the cell, the bit line 241 is connected to ground, while the bit line 242 is connected to the supply voltage V_{CC}. In that

20   case, since neither of the transistors 211,212 conducts, the voltage on the match line does not change, thus confirming that the stored bit matches the looked-for bit. When a logic 0 is being looked for, the bit lines have to be biased in the manner opposite to the previous case, so that this time it will be the transistor 212 that has the low threshold, conducts and therefore tends to reduce the voltage of the match

25   line 230 to ground. When the memorized state is X, neither of the two transistors 211 and 212 can conduct and therefore the looked-for bit and the memorized bit will always coincide.

The operations that have just been described are carried out simultaneously in all the cells of each row of the matrix. When the word contained

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in block 370 is found in a row of the matrix, the voltage of the match line corresponding to that row does not vary and the sense amplifier 380 connected to that match line provides a signal to a priority encoding block 385 that generates an output signal ADROUT that identifies the position in the matrix of the word that

5   corresponds to the looked-for word. Vice versa, when the two words differ by even a single bit, the amplifier 380 detects the voltage variation on the match line and no output signal is generated.

In the described memory matrix, the low threshold of the transistors 211,212 should be accurately controlled to assure that it will always be above a

10   minimum predetermined value, 0.5 V for example. In this connection, let us now consider a matrix cell in which a bit is memorized (*i.e.*, one of the transistors 211,212 has a low threshold). If this cell forms part of a row in which there is no match when the previously described search operation is carried out, the voltage of the corresponding match line will always tend to assume the ground voltage.

15   During the search it may happen that the gate and drain terminals of one of the two transistors 211,212, the one with the low threshold, are at the voltage V_{CC} and that the voltage difference between the gate terminal and the source terminal (connected to the match line) of the same transistor exceeds its threshold voltage when the potential of the match line approaches ground voltage. In that case the

20   transistor under consideration will conduct a parasitic current that charges the match line and increases as the gate-source voltage becomes greater. If several cells in the same row conduct such parasitic currents, the voltage of the match line will not be sufficiently different from its initial pre-charge value (for example, V_{CC}), so that, in a limit case, it may become difficult to detect a non-match during the

25   search. The effect of the parasitic currents can be neglected for the purposes of signal generation on the match line only when the low threshold voltage of the transistors 211,212 is greater than 0.5V. This sets some very restrictive constraints as far as the cancellation algorithm is concerned, which will have to become more and more accurate as the voltage applied to the word line

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diminishes. For example, a voltage of 1.8V on the word line would imply that all the low threshold voltages of all the cells would have to lie between 0.5V and 1V. There still remains the problem of dissipating the power due to the parasitic currents. The worst case occurs when there is a match condition for half the cells

5   in a row and a non-match condition for the other half. The match line voltage comes down to a value intermediate between V_{cc} and ground and a resistive path comes into being between the two potentials.

One should also consider the unfavorable, though not by any means unusual case in which during a search none of the cells of a column of the matrix

10   produce a match, while all the other cells in the matrix are in a match condition; in that case the current passing through one of the bit lines associated with that column has to discharge the capacitances associated with all the match lines of the matrix. In every cell forming part of the column under consideration, indeed, one of the transistors 211 or 212, when conducting, will connect one of the bit

15   lines, which is at ground potential, to the match line of the row that contains the cell that is at the voltage V_{cc}. The match lines to be discharged constitute a relatively high overall capacitive load (for example, 100 pF); in this particular case, therefore, the described matrix will need a relatively long time for carrying out the search operation.

20   When only one cell in a row of the described cell matrix is devoid of a match, the discharge of the match line associated with that row is slower than in the case where a match is lacking in several cells. With a view to speeding up the search operation and also to reduce the dissipation during the switching, the voltage excursion of the match line is reduced by making sure that the voltage of

25   that line will not arrive at ground voltage (starting from the voltage V_{cc}), but rather at low value always greater than ground. This is obtained by using adequate voltage recovery circuits outside the memory matrix and connecting them to the match line during the search. However, the addition of the recovery circuits complicates the circuit structure of the known memory described above.

BRIEF SUMMARY OF THE INVENTION

The disclosed embodiments of the present invention resolve the problems of the known content addressable memory described hereinabove and, more particularly, avoid the limitations imposed on the low threshold voltage of the

5   transistors in order to simplify the cancellation algorithm, render the search operation more rapid, and simplify the circuit structure of the memory.

A non-volatile content addressable memory comprising a multiplicity of memory cells ordered into a matrix of rows and columns, a word line (WL) associated with every row of cells and a first (BLR) and a second (BLL) bit line

10   associated with every column of cells. Every cell comprises a first non-volatile memory element (F1) having a control terminal connected to the word line (WL) associated with the row containing the cell, a first terminal connected to the first bit line (BLR) associated with the column containing the cell and a second terminal connected to a match node (MG) of the cell and a second non-volatile memory

15   element (F2) having a control terminal connected to the word line (WL) associated with the row containing the cell, a first terminal connected to the second bit line (BLL) associated with the column containing the cell and a second terminal connected to the match node (MG) of the cell.

In order to speed up the search for a data item in the memory and

20   simplify the circuit structure of the memory, with each row of cells there is associated a ground control line (GNDCTRL), a ground line (GL) and a match control line (MLCTRL). Furthermore, with every row of cells there is associated a search activation terminal (SF) and a match indication terminal (MPin). Each cell comprises an input terminal (MLIN), an output terminal (MLOUT), a first controlled

25   electronic switch (M0) connected between the input terminal (MLIN) and the output terminal (MLOUT) of the cell and having a control terminal connected to the match node (MG) of the cell, a second controlled electronic switch (M1) connected between the ground line (GL) associated with the row containing the cell and the output terminal (MLOUT) of the cell and having a control terminal connected to the

match control line (MLCTRL) associated with the row containing the cell and a third controlled electronic switch (M2) connected between the match node (MG) of the cell and the ground line (GL) associated with the row containing the cell and having a control terminal connected to the ground control line (GNDCTRL)

5   associated with the row containing the cell.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S)

The present invention will be more clearly understood from the description about to be given of a particular embodiment thereof, which is given purely by way of example and is not to be considered limitative in any way, the

10   description making reference to the attached drawings in which:

Figure 1 shows a circuit diagram of a known non-volatile CAM cell,

Figure 2 shows a circuit diagram of a non-volatile content addressable memory comprising a matrix of cells like the one of Figure 1,

Figure 3 shows a circuit diagram of a non-volatile content

15   addressable memory in accordance with the invention,

Figure 4 shows a circuit diagram of a non-volatile CAM cell in accordance with the invention.

DETAILED DESCRIPTION OF THE INVENTION

As can be seen in Figure 3, the memory in accordance with the

20   invention comprises a multiplicity of cells CELL ordered in a matrix of m rows and n columns. Each row of the matrix includes four electric lines, respectively a word line WL1-m, a ground control line GNDCTRL1-m, a ground line GL1-m, and a match control line MLCTRL1-m, which are connected to a block 10 performing the function of row decoder. Furthermore, the memory includes search activation

25   terminals SF1-m connected to the input of each row of cells and to block 10 and match indication terminals Mpin1-m connected to the output of each row of cells and to sense amplifiers (not shown). Each column includes two lines, a right-hand

bit line BLR1-n and a left-hand bit line BLL1-n, connected to a block 11 performing the function of column decoder and a block 12 performing the function of controlling the search operation. All the cells in the same row are connected to the four lines associated with the row and all the cells in the same column are

5   connected to the two lines associated with the column.

As can be seen from the circuit diagram of Figure 4, each cell includes five transistors: two floating-gate type transistors F1 and F2 that function as non-volatile memory elements and three transistors M0, M1 and M2 that act as electronic switches. The two transistors F1 and F2 have their source terminals

10   connected to a common electric terminal MG that will henceforth be referred to as a match node, their gate control terminals both connected to a word line WL and their drain terminals connected, respectively, to a right-hand bit line BLR and left-hand bit line BLL. The transistor M0 of each cell has its gate terminal connected to the match node MG and its source-drain section connected between an input

15   terminal MLIN and an output terminal MLOUT of the cell. The transistor M1 has its gate terminal connected to a match control line MLCTRL and its source-drain section connected between a ground line GL and the output terminal MLOUT. The transistor M2 has its gate terminal connected to a ground control line GNDCTRL and the source-drain section connected between the match node MG and the

20   ground line GL.

The transistors M0 belonging to cells of a same row are connected in series to each other in such a way that the output terminal (MLOUT) of each cell (excluding the last) is connected to the input terminal (MLIN) of the next cell of the row and the input terminal of each cell (excluding the first) is connected to the

25   output terminal (MLOUT) of the previous cell of the row. The input terminal (MLIN) of the first cell of each row is connected to the search activation terminal (SF) of the row and the output terminal (MLOUT) of the last cell of each row is connected to the match indication terminal (MPin) of the row

In each cell, similarly to the case of U.S. Patent No. 6,317,349 B1, when a low threshold is fixed for F2 (for example, 1V) and a high threshold for F1 (for example, 5.5V), a logic 0 is memorized, while a logic 1 is memorized when the thresholds are set in the opposite manner. When both threshold are programmed

5   with a low value, the don't care state X is memorized. The proposed cell therefore also constitutes a ternary content addressable memory.

To write a bit into a CAM cell like the one of Figure 4 that has already been cancelled (transistors F1 and F2 with low thresholds), a high voltage is first applied to the word line WL (for example, from 5V to 8V). If the voltage of the

10   ground control line GNDCTRL is set at a high value (for example, 5V to 8V) and the ground line GL is maintained at ground potential, thus enabling transistor M2 to conduct, the match node MG will likewise be connected to ground potential. To memorize a logic 1, an intermediate voltage is applied to the left-hand bit line, leaving the right-hand bit line BLR unconnected. Therefore the threshold of

15   transistor F2 increases and the threshold of transistor F1 remains low. When a logic 0 is to be memorized, one acts in the opposite manner on the bit lines to step up the threshold of transistor F1. A low voltage remains on both the bit lines when the don't care state X is to be memorized.

When a bit in the cell is to be cancelled, the substrate of the

20   transistors F1, F2, common to all the cells, is fixed at a high voltage (for example, 8V), a negative voltage is applied to the word line WL (for example, from −7V to − 9V) and the ground control line GNDCTRL and match control line MLCTRL are connected to ground, leaving the other lines unconnected. In this way the electrons are removed from the floating gate of the transistor of the pair F1,F2 that

25   has the high threshold, while the threshold of the other is altered to a far lesser extent.

With a view to describing the search operation, matters can be simplified by analyzing the functioning of a cell forming part of the first column of the matrix shown in Figure 3 (all the cells of the matrix function in a similar

manner). In this cell, ground potential (V_{GL}) is initially applied to the ground line GL, while a sufficiently high voltage (for example, from 5V to 8V) is applied to the ground control line GNDCTRL and the match control line MLCTRL in order to cause the transistors M2 and M1 to conduct; the node MG and the output terminal

5 MLOUT will thus become discharged and assume the voltage of the line GL, i.e., ground potential. Furthermore, the block 10 applies a voltage V_{SF} (comprised between 0.5V and the supply voltage of the integrated circuit of which the memory forms part, for example, from 1.8V to 3V) to the search activation terminal SF of the row in which the cell is situated: in this particular case, the search activation

10 terminal SF is connected to the input terminal MLIN of the cell under consideration.

It is assumed that this cell stores a logic 0 (F2 with low threshold, F1 with high threshold). When the bit to be sought in the cell is a 1, a voltage V_{SEARCH} (for example, from 1.2 to 2V) is applied to the right-hand bit line BLR and the left-hand bit line BLL is left unconnected. Setting an appropriate voltage, greater than

15 the low threshold voltage of the transistors F1 and F2, (for example, 4V) on the word line WL and applying ground potential to the ground control line GNDCTRL and the match control line MLCTRL in order to shut down the transistors M2 and M1, neither of the transistors F1 and F2 will conduct, the match node MG is not charged, and the transistor M0 remains off. Consequently, the voltage V_{SF} applied

20 to the input terminal MLIN cannot become transferred to the output terminal MLOUT. The stored bit does not match the bit that is being sought and is therefore a 0. Vice versa, when the looked-for bit is a 0, the same voltage V_{SEARCH} is applied to the left-hand bit line BLL, leaving the right-hand bit line BLR unconnected. In that case transistor F1 remains off, while transistor F2 conducts

25 and causes the voltage of the internal node MG to increase to the value V_{SEARCH}. This voltage causes the switching on of the transistor M0; consequently, the node MLIN becomes connected to the node MLOUT and the voltage V_{SF} becomes transferred. The stored bit matches the bit that is being sought and is therefore a 0.

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Referring to the cell matrix shown in Figure 3, during the search for a binary word stored in a register contained in block 12, block 11 applies the voltage V_{SEARCH}, which it receives from a regulator (not shown), to one of the bit lines of each of the n pairs (leaving the other bit line unconnected), while block 10 sets the

5   voltages on the word lines WL1-m, the ground lines GL1-m, the ground control lines GNDCTRL1-m, and the match control lines MLCTRL1-m of each of the m rows. The block 10 also sets the voltage V_{SF} on the search activation terminals SF1-m of the m rows. The voltages considered so far are in practice voltage pulses of predetermined duration which are applied to the electrical lines of the cell

10   matrix, both to the rows and the columns, in predetermined times by an appropriate clock signal. In particular, the voltage V_{SF} applied to the search activation terminals SF1-m is a voltage pulse. When there is a match between the word memorized in a row and the word that is being looked for, this voltage pulse becomes transferred from the first to the last cell of the row, *i.e.*, from the search

15   activation terminal to the match indication terminal, where it is detected by a sense amplifier. However, the array of transistors M0 of each row, besides to reduce the pulse amplitude, modifies the pulse leading edge by reducing its slope.

When the number of cells in each row is particularly high, the above mentioned effect can become heavy and the leading edge is flattened until it

20   cannot be detected with certainty by the sense amplifier. In this case, in certain applications it may be advisable to introduce one or more buffers at regular intervals in the series connection of transistors M0 of the same row in order to restore the slope of the leading edge of the pulse. When the word memorized in the row does not match the looked-for word by even a single bit, the voltage V_{SF}

25   cannot become transferred and therefore the amplifier does not detect any voltage variations. When the state memorized in a cell of the row is the don't care state X, the two transistors F1 and F2 of the cell conduct, the voltage V_{SF} becomes transferred, and there will thus always be a match. The voltage on the node MG

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and the output terminal MLOUT is discharged at the end of each search operation, thus re-activating the transistors M2 and M1.

The above description of the memory makes it clear that the transistors M0 forming part of cells that are situated in the same row of the matrix are connected in series with each other. Bearing in mind both this circuit arrangement and the functioning of the cells during the search, each row of the matrix performs during the search the logic function of an AND gate that has the n MG nodes as its inputs and the match line indication terminal MPIN as its output. In fact, if the voltages that can be assumed by the node MG of each cell, i.e., the voltage V_{SEARCH} (when there is a match) and ground potential (when there is no match), are interpreted, respectively, as logic 1 and logic 0 and the states of variation of the voltage and non-variation of the voltage of the terminal MPin are interpreted, respectively, as logic 1 and logic 0, a logic 1 on the output side of the gate will be obtained only when all the inputs are 1, according to the logic of an AND gate. For this reason, the memory in question can be called an AND-type content addressable memory.

During the search the match node MG of each individual cell is not connected to the match nodes MG of the cells situated on other columns, but by means of the bit lines BLR and BLL is connected only to the match nodes MG of any cells in a matching state forming part of the same column.

It is easy to note that the present disclosed embodiment of the invention has numerous advantages as compared with the prior art. In particular, in the unfavorable case, in which all the cells of a matrix column according to Figure 3 are in a matching state, that is equivalent to the case considered in connection with U.S. Patent No. 6,317,349 B1, in which all the cells of a matrix column are in the non-matching state, the currents in the bit lines will charge only the nodes MG of the cells on the same column, so that they will charge an overall capacitance having a much smaller value than the capacitances that have to be

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discharged – all other conditions being identical – in the case of the memory of Figure 2, *i.e.*, the capacitances associated with all the match lines of the matrix.

According to the invention, the source terminals of the transistors F1 and F2 of every cell (coinciding with the respective nodes MG) are not directly

5   connected to the match line, *i.e.*, to the line that provides the series connection for the transistors M0 and corresponds to the match line ML of Figure 1. When a logic 1 or a logic 0 is memorized in a row (all the cells with at least one of F1 and F2 having a high threshold), parasitic currents cannot be produced. These currents are generated only in rows of which the content has been cancelled (F1 and F2

10   with a low threshold) and can be eliminated by bringing the corresponding word lines to a low voltage (for example, from ground potential to –2V). In each case the parasitic currents will – at the very worst – charge the MG node and not the respective match line. Consequently, erroneous non-match valuations are avoided, the search is completed more rapidly, and the low threshold of F1,F2

15   does not have to be accurately controlled, thus simplifying the cancellation algorithm.

Although only a single embodiment of the present invention has here been illustrated and described, it is clear that numerous variants and modifications are possible without overstepping the inventive concept. For example, the block

20   11 could be designed in such a way that during the search the bit lines of every column are biased to, respectively, a voltage of V_{SEARCH} and ground potential rather than one at the voltage V_{SEARCH} and the other without any potential (because left unconnected or connected to a high-impedance terminal). In this way one avoids having to use a three-state device for biasing each pair of bit lines

25   that would otherwise be necessary in order to have a high-impedance state. Furthermore, the initial value of the voltage of the MG node needs not be set to ground potential, but could be a positive voltage (1.8V, for example). In that case the voltage V_{SEARCH} (which charges this node when there is a match) has to be higher, but one obtains the advantage of reducing the voltage excursion of the

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node MG and the dissipations associated therewith. Lastly, at the beginning of the search the voltage of the output terminal MLOUT of each cell can be set to a pre-charge value of 1.8V (rather than ground potential). In that case the negative voltage V_{SF} is applied to the search activation terminal to drive transistor M0

5 correctly and, this time, a pulse is transferred with trailing edge.

All of the above U.S. patents, U.S. patent application publications, U.S. patent applications, foreign patents, foreign patent applications and non-patent publications referred to in this specification and/or listed in the Application Data Sheet, are incorporated herein by reference, in their entirety.

10 From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.